國立清華大學
專題研究報告

National Tsing Hua University
Independent study

N+/P 殼狀混合式多晶矽無接面場效電晶體

N+/P Hybrid Poly-Si Shell Structure Junctionless Field-Effect Transistors

系別：工程與系統科學系

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Abstract

Nowadays, electronic products tend to the trend of low power consumption, low cost and small size. Because of the products miniaturization, the short-channel effects and physical limitations will be a challenge for conventional transistors. However, the birth of junctionless transistors has been reduced above problems probably. The characteristics of the junctionless transistor is that the source, drain and the channel doping have all the same type and concentration, and because no junction exists between the channel and S/D, the junctionless transistor is called. Junctionless transistor not only reduces the thermal budget of the process, but also suppresses the short-channel effects. It is one of the novel structure worth noting in the future.

This work proposes the N^+/P hybrid poly-Si shell structure junctionless field-effect transistors with N^+ insitu-doping on the p-type substrate. We adjusted the exposure dose to reduce the process flow and time, and we used the same mask to complete the N-channel and P-type substrate etching step. In order to turn-off the JL-FET architecture, the multi-gate structure and ultra-thin body (UTB) are the candidate to achieve the full depletion region at off-state. It can improve the switching capability of the device to reduce leakage current and power consumption. Since the depletion region formed between N^+ channel and p-type substrate interface, it is used to reduce channel thickness (Tch) and turn off the device more easily.

This work exhibits the N^+/P hybrid poly-Si shell structure junctionless field-effect transistors. The NW shell JL-FET exhibits the superior electrical properties, including high ON/OFF current ratio (>5×10^6), steep subthreshold swing (95 mV/dec.) and low value of Drain Induced Barrier Lowering (50 mV/V). We also discuss the electrical characteristics of this device at high temperatures. In the last part, we use Sentaurus TCAD simulation software to analyze this device, and compare the simulation results with the experimental data.

The N^+/P hybrid poly-Si shell structure junctionless field-effect transistors has excellent electrical characteristics and is simple to process, so it has tremendous potential application on low-power devices and three-dimensional stack structures in the future.

I. Introduction of junctionless transistor

Conventional inversion- mode (with junction) are difficult to fabricate, and because they occur a significant source of current leakage, result in wasting a lot of power consumption. The junctionless means there are no junction between the S/D region and channel (shown in figure1). Junctionless transistor is not turned off by reverse bias voltage applied to the gate, but by full depletion of the channel. This depletion is formed due to work-function difference between the gate material and doped polysilicon. The current drive is controlled by doping concentration but not by gate capacitance.

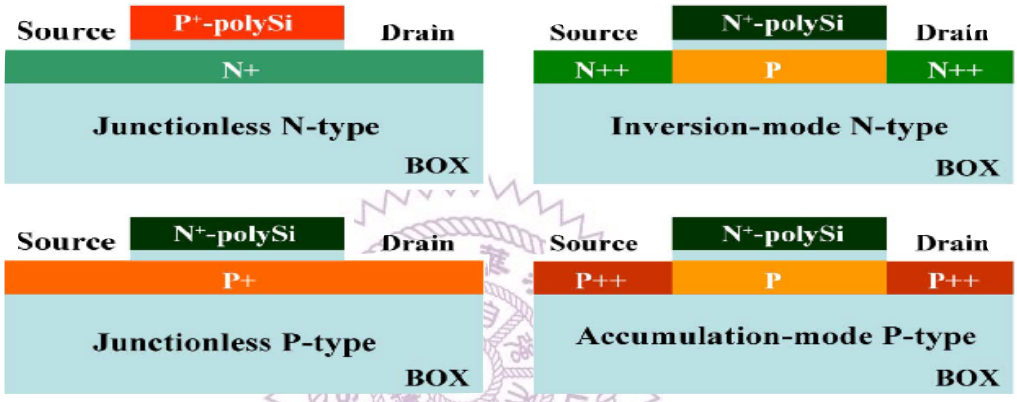
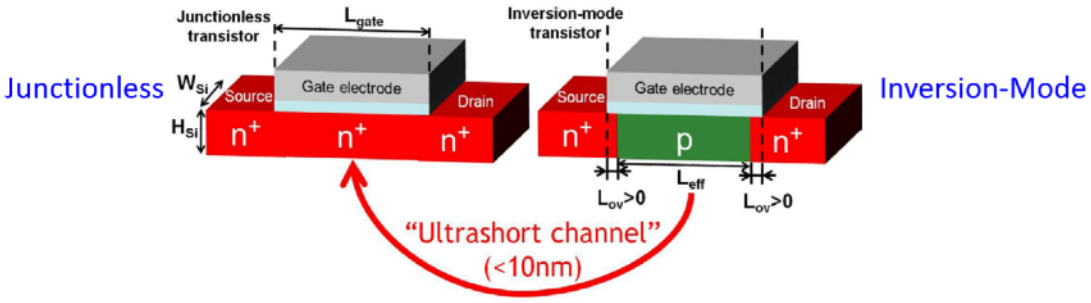


Figure 1. The cross-sectional view of JL NMOS, JL PMOS, IM NMOS and accumulation- mode PMOS silicon nanowire FETs [1-2]



Advantage of JL-FET：

1. Avoid the formation of ultra-steep S/D profiles → reduced the SCE

2. Process easier than IM-Mode

3. Body current → reduced the surface scattering

Figure 2. Advantage of JL-FET

II. Fabrication flow

In this study, the N^+/P Hybrid Poly-Si Shell Structure Junctionless Field-Effect Transistors (N^+/P Shell JL-FET) was fabricated. Figure 3-1 shows the structure of N^+/P hybrid Shell JL-FET and the device with ten nanowires (NWs) channel. The key process flow of fabrication in this work are presented in figure 3-2, and the cross section diagram is along the gate direction.

The process steps of this device is following:

Step1. Solid-phase recrystallized (SPC) process

First step, a 400 nm-thick thermal SiO_2 layer on 6 inches silicon wafers as buried oxide. Then, a 50 nm-thick undoped amorphous -Si (α-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C and then the α-Si layer was solid-phase recrystallized (SPC) at 600 ^oC for 24 hours, in order to form large grain size in nitrogen ambient atmosphere.

Step2. P-type substrate formation

Continue in the previous step, the 50 nm-thick undoped α-Si layer was implanted with 32-keV boron (BF_2) ions at a dose of 2×10^{14} cm^{-2}, and then annealed by furnace at 600^oC for 4 hours. Next, deposit 40 nm dry-oxide and dilute HF to reduce the 50 nm p-type layer become almost 17 nm, this method called oxide trimming. Afterwards, p-type substrate layers with ten nanowires (NWs) were defined by electron beam lithography (EBL) and time-controlled reactive-ion etching (RIE). By the way, the e-beam lithography exposure with dosage = 5.0 $\mu C/cm^2$.

Step3. In-situ N^+ doped poly-si & hybrid shell structure formation

In this step, we divided into two kinds of experimental structures, included NW Shell and Planar Shell. The 18 nm-thick N^+ polysilicon in-situ doped above the p-type substrate layer and the N^+ polysilicon layer is regarded as channel.

In the NW Shell structure, E-beam lithography (EBL) exposure again with the same mask as the p-type substrate layer but different dosage (5.6 $\mu C/cm^2$) and then etched by RIE to form the ten hybrid NWs. Furthermore, another structure called Planar Shell, this is also performing the same process but using a larger dosage (6.8 $\mu C/cm^2$) of EBL exposure. After reactive-ion etching (RIE), the N^+/P hybrid planar shell structure are defined (shown in Fig 3-3 and Fig 3-4).

Step4. Gate electrode formation

Moreover, 10 nm-thick thermal oxide was deposited by LPCVD as the gate oxide layer, consume about 10 nm-thick N^+ polysilicon to form 8 nm-thick channel. Afterwards, 150 nm-thick in-situ doped N^+ polysilicon was deposited as a gate electrode and got patterned by e-beam lithography (EBL), etched by end-point mode RIE.

Step5. Passivation and metallization formation

A 200 nm-thick Tetraethyl Orthosilicate (TEOS) oxide layer was deposited as passivation by LPCVD. Furthermore, the contact window was defined on the passivation layer and the window curve was filled with 300 nm-thick Al-Si-Cu. Eventually, all wafer sintered at 400^{o}C for 30 minutes in hydrogen ambient to repair interface dangling bond.

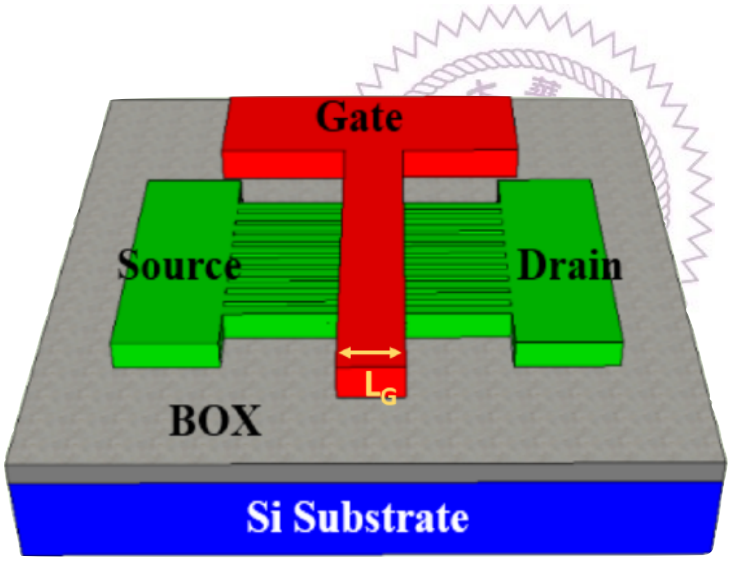


Figure 3. Scheme of the N^+/P hybrid shell JL-FET

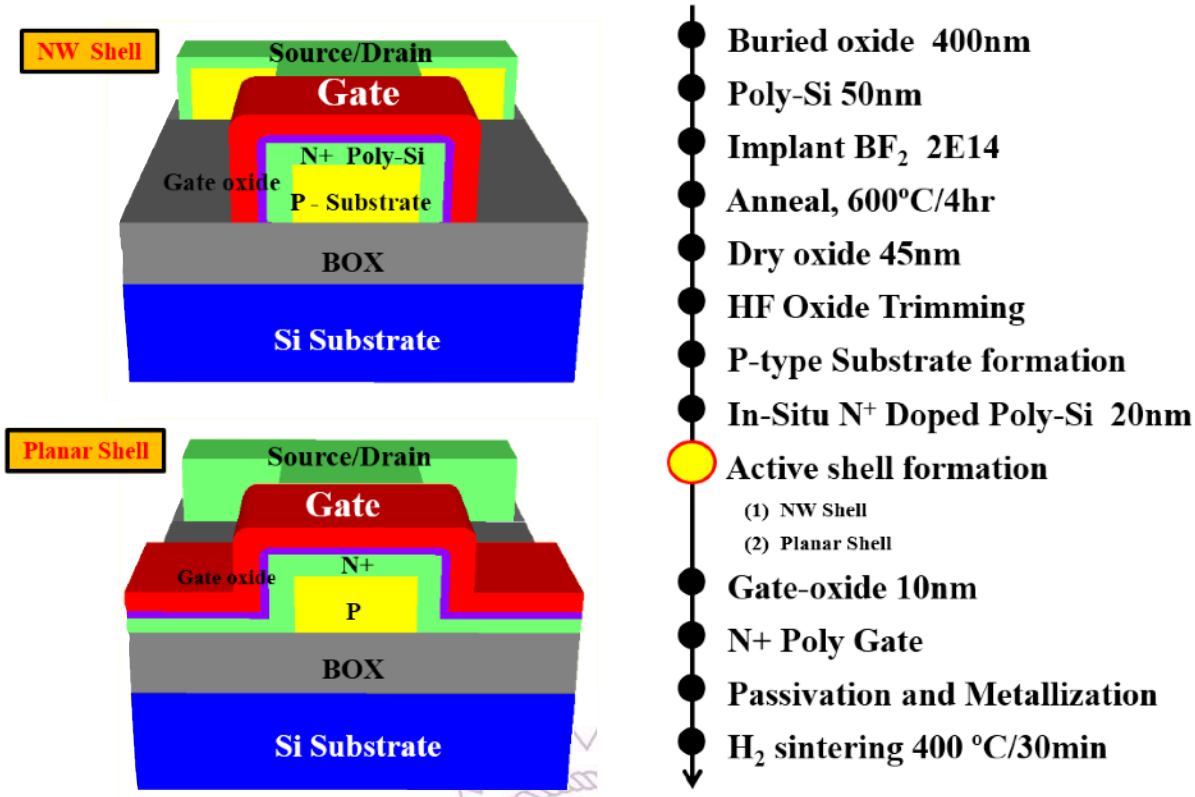


Figure 4. The key process flow of N+/P hybrid shell JL-FET and the cross section of schematic (NW Shell and Planar Shell included) along the gate direction

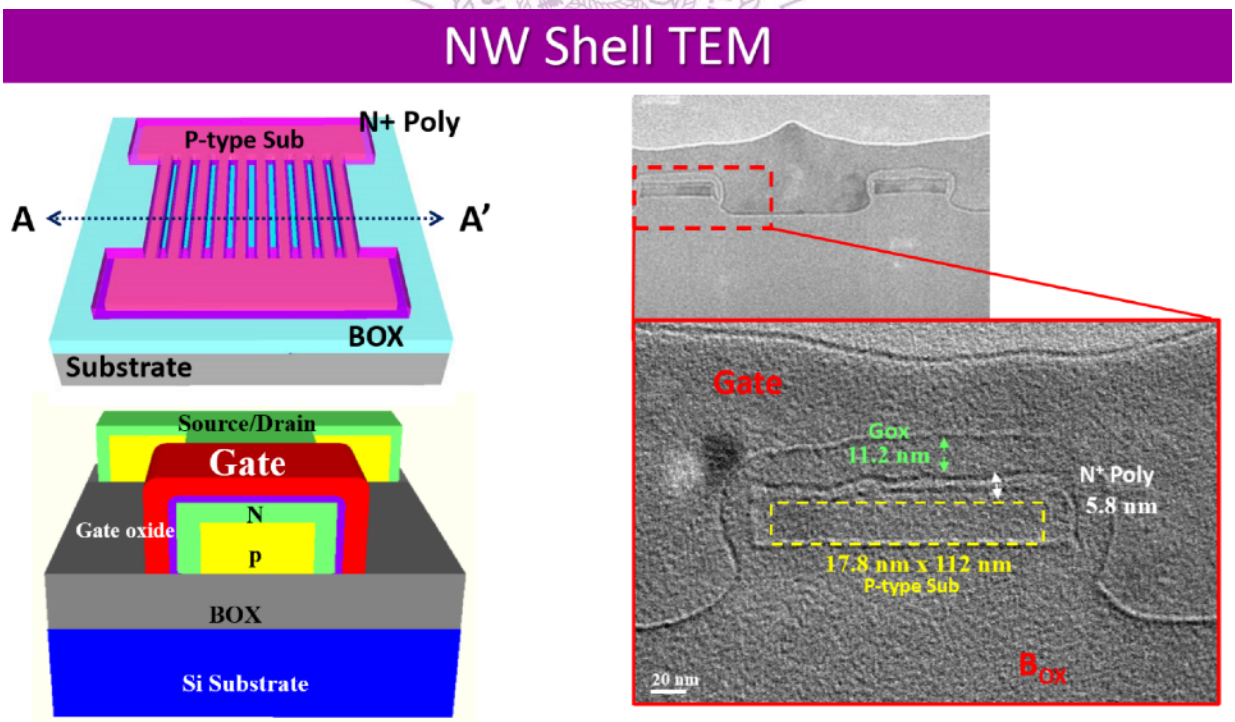


Figure 5-1. NW Shell TEM

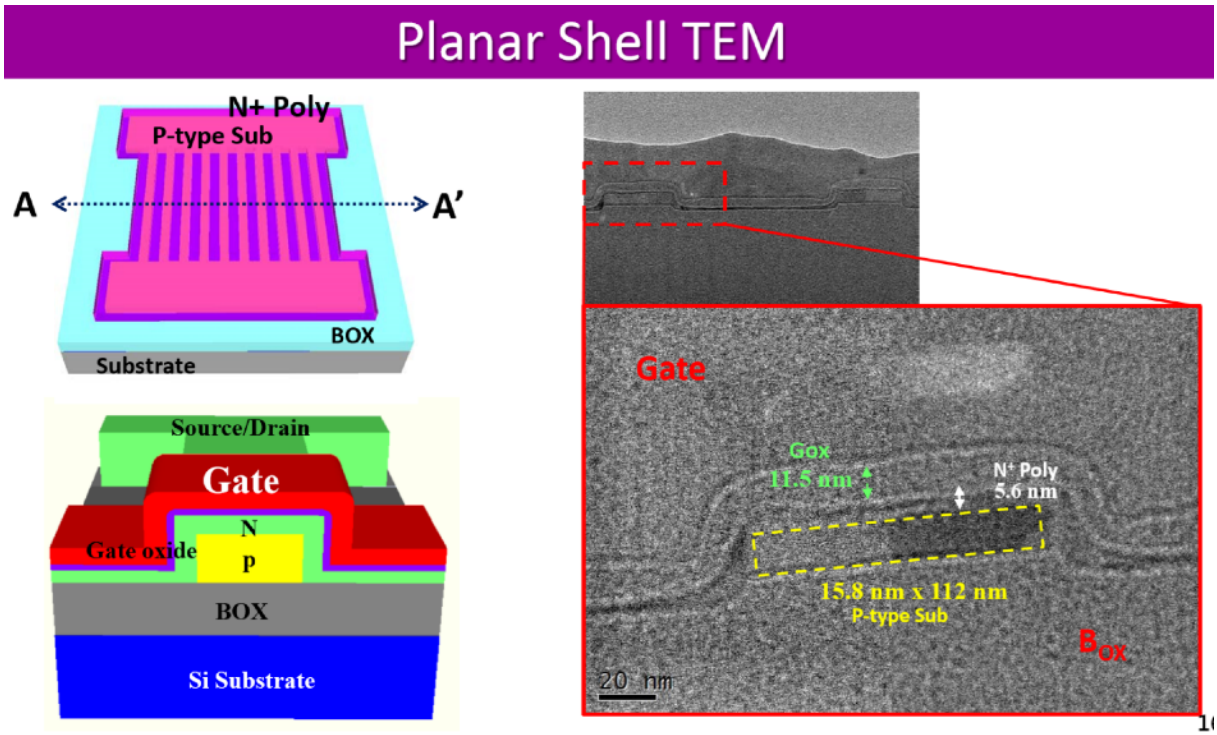


Figure 5-2. Planner Shell TEM

III.Result and discussion

Device Electrical Analysis

Figure 6-1 shows the plots of I_D–V_G characteristics of NW shell JL-FET and planar shell JL-FET at V_D = 1 V. The on current of NW shell JL-FET have slightly higher than planar shell JL-FET and off current of NW shell JL-FET is obviously lower than planar shell JL-FET. The device current have been normalized by dividing W_{eff} to compare device performance precisely. The below plot of figure6-2 is linear scale of I_D–V_G curve, it shows the NW shell JL-FET have higher saturation current. The NW shell JL-FET have threshold voltage (V_{TH}) = 0.24 V and the planar shell JL-FET is 0.39 V, where V_{TH} is extracted at $I_D = 10^{-8}$ A by constant current method.

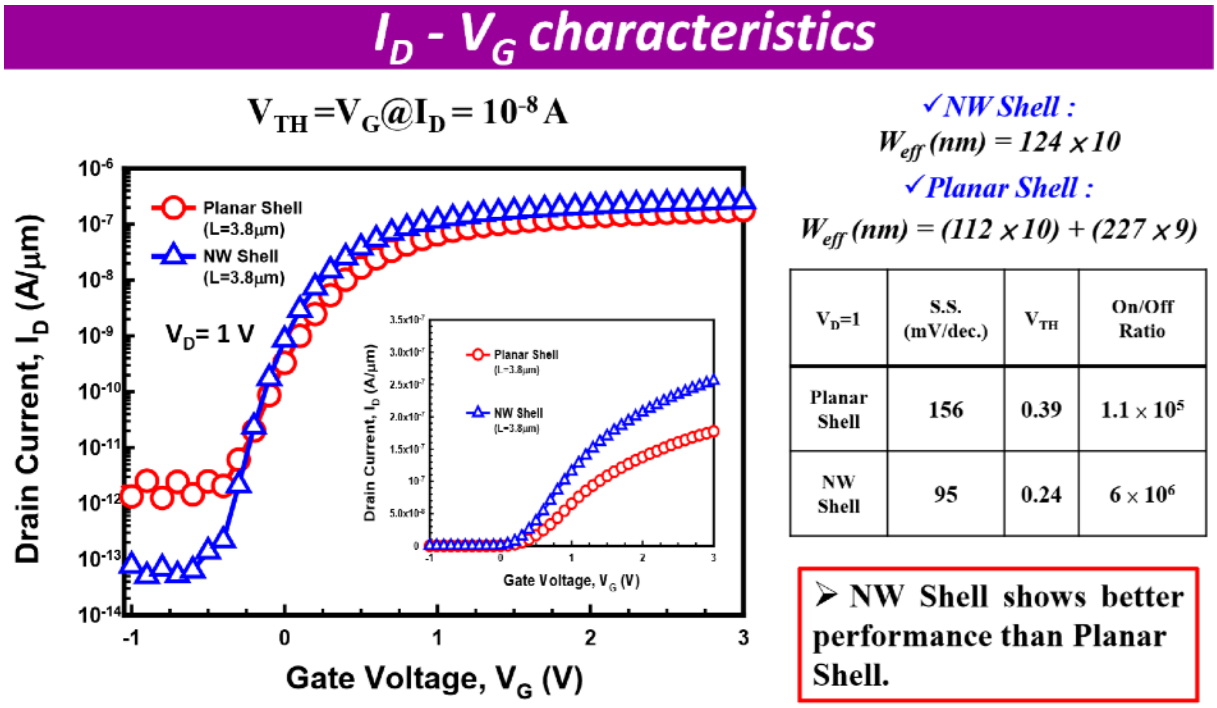


Figure 6-1. I_D–V_G characteristics of NW shell and planar shell JL-FET at V_D = 1 V

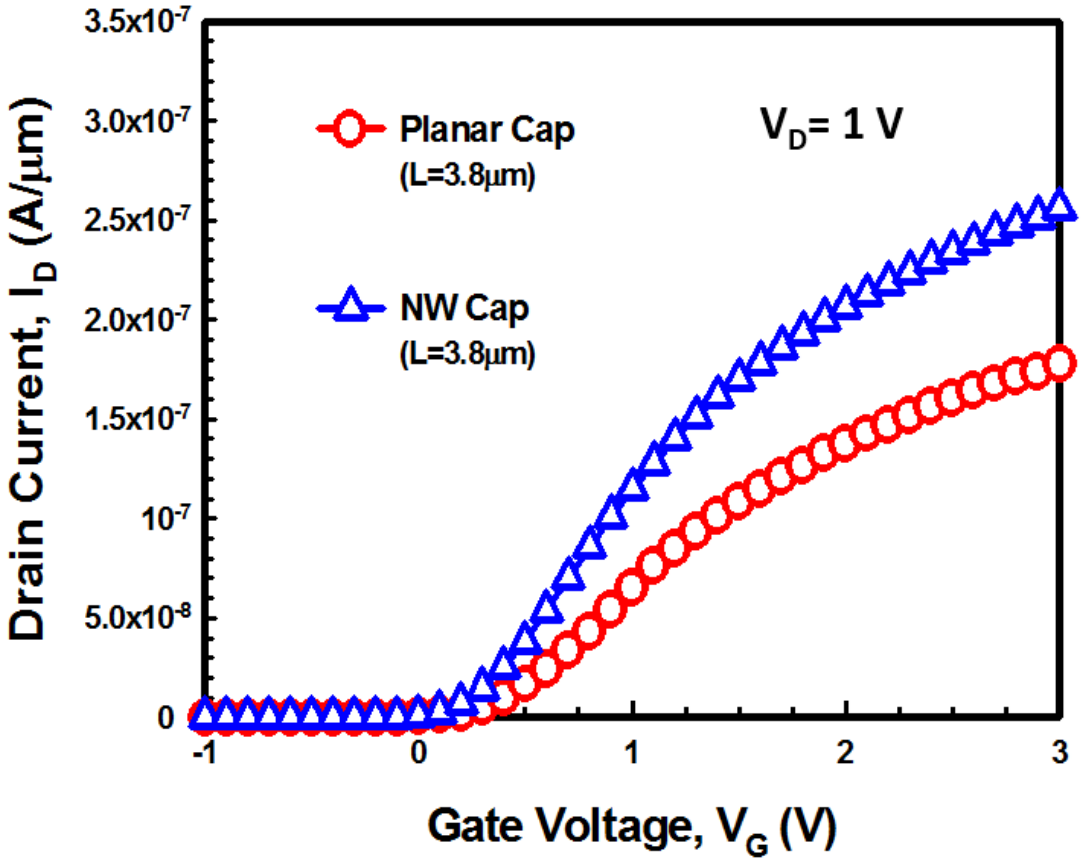


Figure 6-2. Exhibits I_D–V_G characteristics of NW shell JL-FET and planar shell JL-FET with L_g = 3800 nm at V_D = 1 V. The NW shell JL-FET has the better performance and higher ON/OFF current ratio than planar shell JL-FET. The below figure is linear scale of I_D–V_G curves.

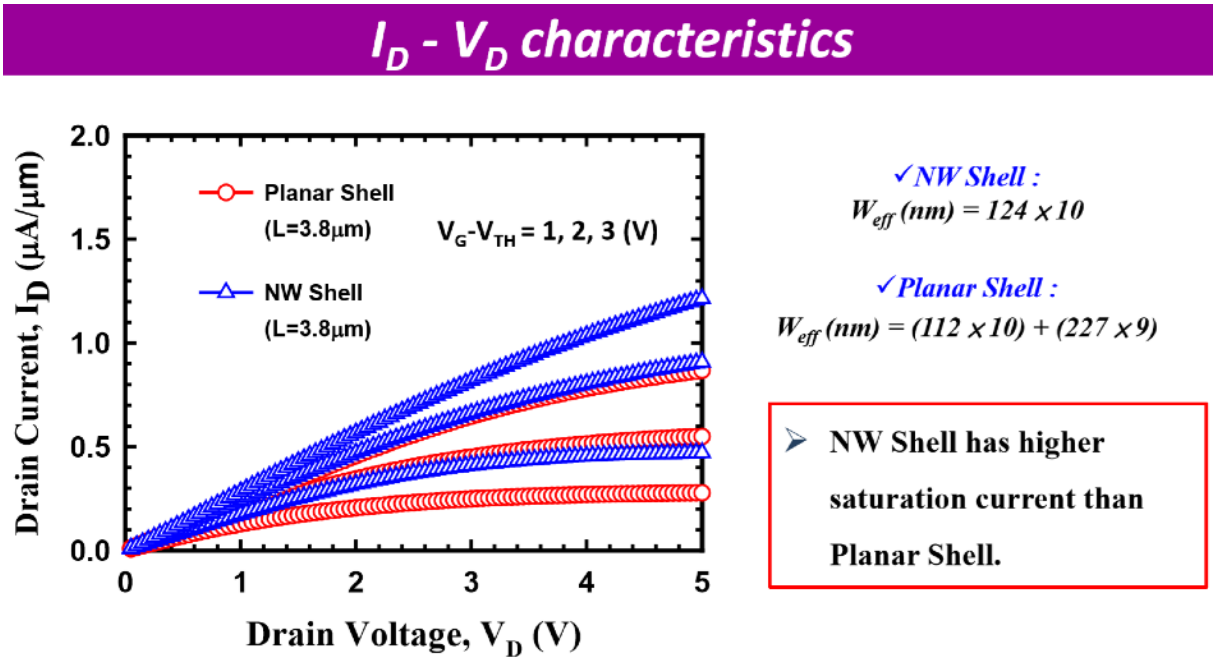
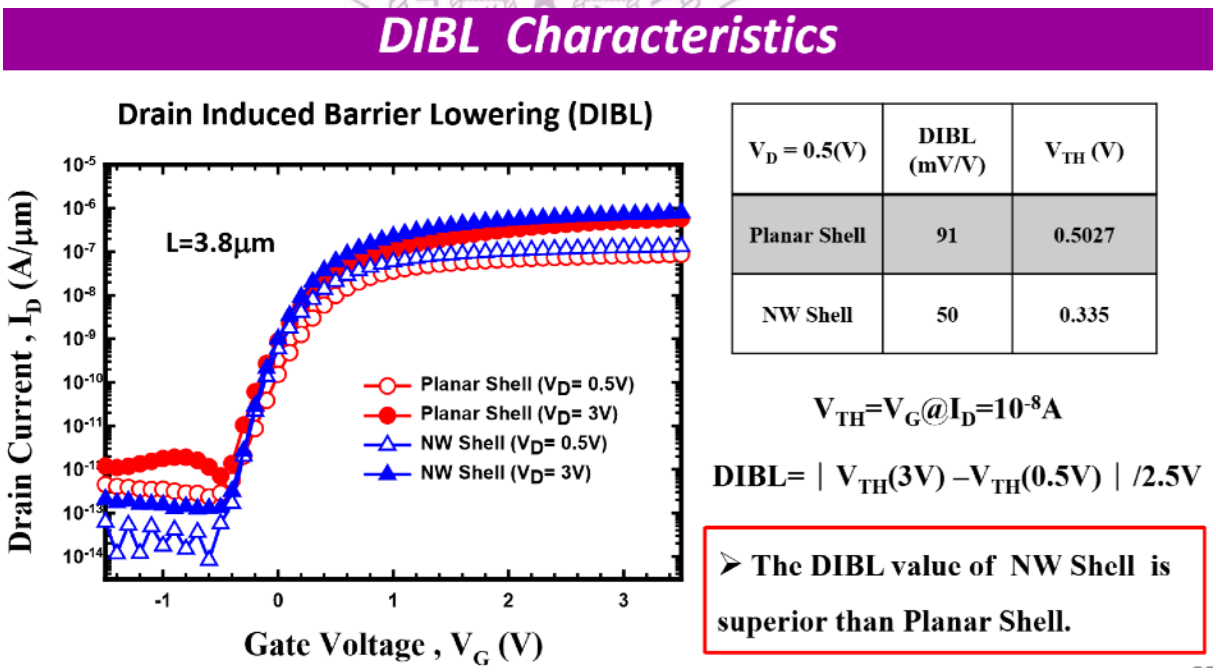


Figure 7. The I_D–V_D curves of NW shell JL-FET and planar shell JL-FET, also exhibits NW shell saturation current around 1.5 times higher than planar shell at V_G-V_{TH} = 3, V_D = 5V. Because the NW shell JL-FET has superior gate control ability.



V_D = 0.5(V)	DIBL (mV/V)	V_{TH} (V)
Planar Shell	91	0.5027
NW Shell	50	0.335

Figure 8. Compares the I_D-V_G curves between the NW shell JL-FET and planar shell JL-FET at V_D = 0.5 V and V_D = 3 V. V_{TH} is defined as the gate voltage at I_D = 10^{-8} A. And also display the drain induced barrier lowering values of NW shell JL-FET (DIBL = 50) is lower than the planar shell JL-FET (DIBL = 91). The DIBL value is derived from the V_{TH} at V_D = 0.5 V、3 V.

Conclusion

In order to turn off the junctionless transistors, we use the tri-gate structure to achieve the full depletion region at off-state. We adopted hybrid N^+ channel and p-type substrate structure to form the depletion region, and it is used to reduce the effective N^+ channel thickness (Tch) and turn off the device more easily.

The N^+/P hybrid poly-Si shell structure junctionless field-effect transistors were successfully fabricated and characterized. We also adjusted the exposure dose to finish the channel/substrate etching and reduce the process flow. SEM and TEM analysis confirmed that the N^+/P hybrid JL-FET has a clear PN junction, the N^+ channel which the major carriers flow path is 5.8 nm-thick and the P-type substrate is 17.8 nm-thick. The performance of the NW shell JL-FET is superior with the steep sub-threshold swing (95mV/dec.), the high current ratio (I_{on}/I_{off} current ratio > 5×10^6) and DIBL (50mV/V). Furthermore, the reliability of the device is proved by the temperature-dependence electrical characteristic with variable temperature with 25^oC per steps from 50 ^oC to 200 ^oC. The NW shell JL-FET is much less sensitive to temperature than the planar shell JL-FET, so the NW shell JL-FET is convenient for circuit design with using in a wide range of temperatures. The proposed N^+/P hybrid JL-FETs with shell structure are not only easy to fabricate but also has excellent characteristics for advanced low-power consumption and three-dimensional stack structures in the future.

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